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Power Consumption Technique to Improve the Network Life Time in Wireless Sensor Networks

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Abstract

Phase/frequency detector has two outputs as up and down pulses. These two pulses are used to drive charge pump and to convert them into analog quantities to control the voltage control oscillator in PLL. The objective of this paper is to implement the Charge Pump circuit with 9 MOS transistor with 180nm CMOS technology operated with low supply of 0.5V only and to reduce the overall circuit power. In IC technology which is powered by battery, if the total power dissipation is low, the service time offer by the battery is longer. This work mainly aim at the reduction of power dissipation with low voltage supply.

Keyword: Charge pump; charging; saturation; current source; W/L ratio; Control voltage; spur.

Introduction

Much work has been reported on charge pump circuit with different voltage supply. With reference to [1] a circuit is already design with 2V using positive feedback for increasing the switching speed and to reduce the spur. The paper presented here is to reduce the supply voltage so that the overall power dissipation is also reduced. All PLL components is presented well and a charge pump is simulated with 0.7V [2]. A charge pump consists of two switched current sources as shown in Fig2 that pump charge into or out of the loop filter according to the two logic inputs up and down. A charge pump is basically driven by a PFD and it again drives a load capacitor.

Basically it manipulates the amount of charge on the filter's capacitor depending upon the signals from the UP and DOWN outputs of the PFD. The phase frequency detector (PFD) detects phase or frequency differences, and activates the charge pump accordingly. In PLL when the loop is turned on, ωout of VCO may be far from ωin at the PFD input. This frequency or phase difference is detected by the PFD and converted into proportional output voltage by the charge pump to vary the control voltage of VCO such that ωout approaches ωin. When the input and output frequencies are sufficiently close, the PLL is in lock phase [3]. The loop locks when the phase difference drops to zero and the charge pump remains relatively idle.

Charge Pump

Based on the applications different types of charge pump is already presented. Some types are built so that it gives output higher than the supply voltage using Dickson charge pump [5], [6]. The charge pump here is another class which form a basic block of PLL which varies its output only up to the supply voltage for controlling a very sensitive VCO. Charge pump is the circuit that translates the UP and DOWN signals from the PFD to control voltage that will control the VCO. As shown in figure, charge pump consist of two controlled switches UP and DOWN to charge and discharge the capacitor. According to the two signal level, current sources driving a load capacitance at the output will give control voltage to the voltage control oscillator [4]. Charge pump stabilizes spurious fluctuation of currents and switching time, to minimize the Spurs in the VCO input.

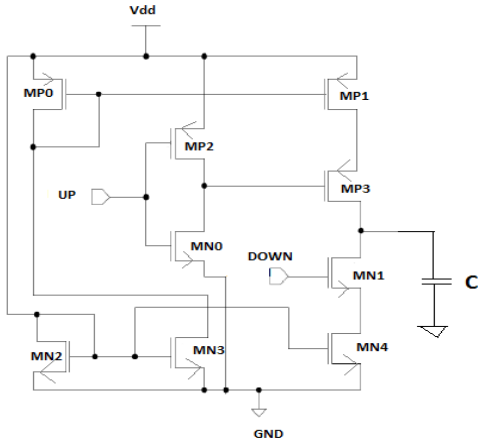

Fig 1. Transistor Level Charge pump circuit diagram

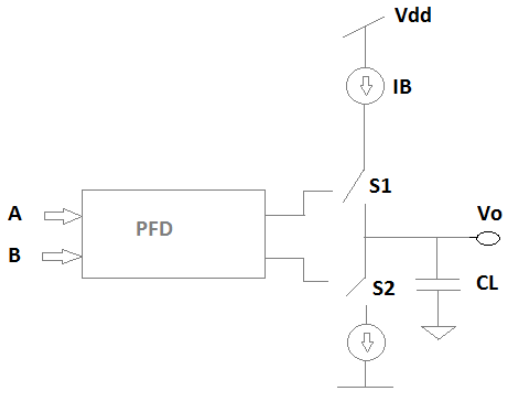

Fig2. PFD driving charge pump

The table shown below is the operation that takes place in the charge pump for both, different value and same value of UP and DOWN pulse

UP	DOWN	Description
1	0	IB deposit current in CL raising Vo
0	1	IB sink current from CL reducing Vo
0	0	Both switches are off and no Vo changes

When the up signal is activated the switch S1 is closed and the capacitor start charging gradually. But when the down signal is activated the capacitor discharge down to ground level through switch S2 close path. If the loop is locked PFD detect no phase difference and the control voltage of VCO remain unchanged and constant. This is the case when both the switch S1 and S2 are open.

Simulation Result

Simulation is carried out with a pulse train of 5 MHz with duty cycle 50 % having on time of 100ns and off time of 100ns. The amplitude of the pulse is 0.5 V with rise time and fall time of 1psec each. By activating the up pulse high the timing output voltage across the capacitor is slowly rising for each high pulse as shown below in fig 3.

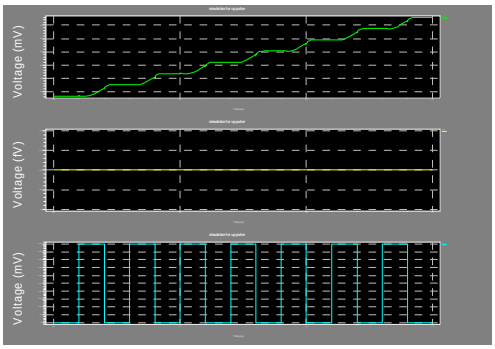

Fig 3. Charging up load capacitor

Again by activating the DOWN pulse high and keeping the UP pulse low the simulation obtained is as follow, that is the charge across the capacitor is discharging

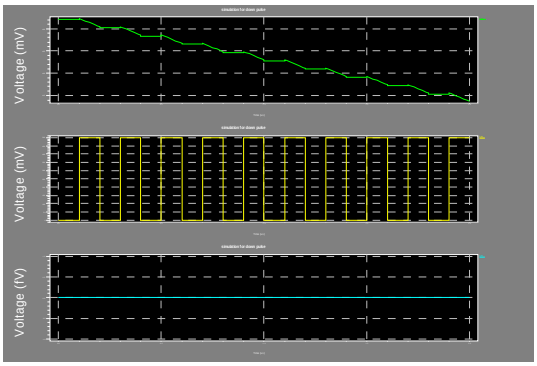

Fig 4. Discharging of capacitor

By increasing the simulation length for both UP and DOWN pulse, the capacitor charge reaches its final value and ground state respectively as shown in the simulation result below. To discharge it takes almost 6µsec the same time as saturation time.

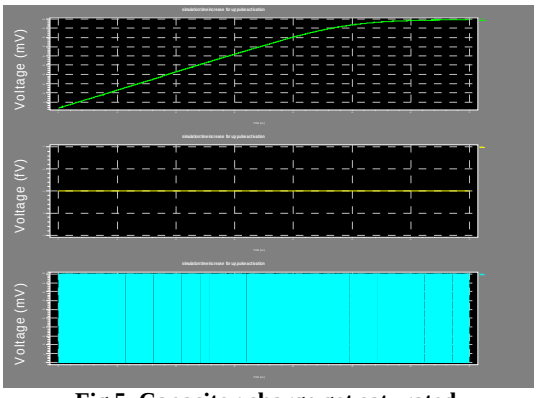

Fig 5. Capacitor charge get saturated

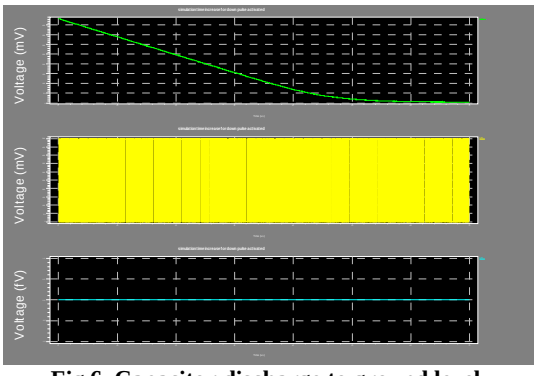

Fig 6. Capacitor discharge to ground level

When both the driving signals are on and off alternately, the capacitor charge and discharge respectively as shown below in the simulation result.

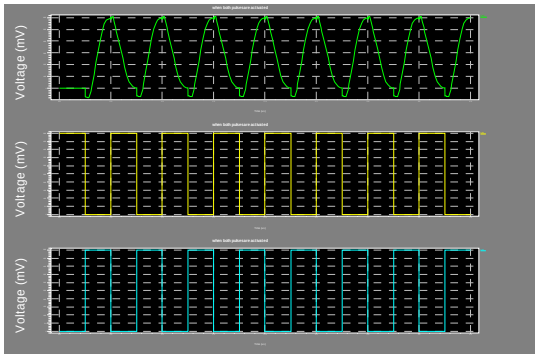

Fig 7. Control voltage is not constant when PFD detect complete phase difference between the activating signals.

All simulation results of the charge pump circuit is listed in Fig 8.

Design result

Technology use	CMOS 180nm
supply voltage	0.5 V
total circuit current	3.54 uA
power dissipation	1.77 uW
load capacitance	6 pf
W/L for NMOS and PMOS	5/19 and 2/15
saturation time	6 usec
desaturation time	6 usec
Rate of charge and discharge	0.083mV/1us
toll use	Tanner Spice

Fig 8

The charging rate of the capacitor is linear before it reaches its saturation state. At 6 usec it is fully charge up to the supply voltage as shown in fig 8. The discharging rate is also same as charging rate.

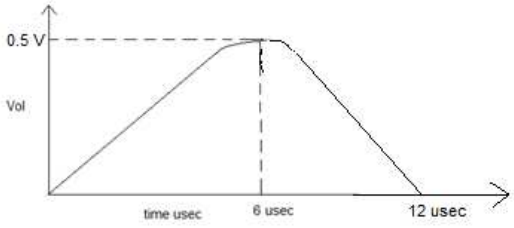

Fig 9. Rate of rise and fall of capacitor voltage at 0.083mV/1usec .

Conclusion

This low voltage charge pump is implemented by precisely optimising the (W/L) ratio without affecting the overall performance. The driving pulse from the PFD is of 0.5V. The overall circuit current is 3.54uA and power is 1.77uW. The overall performance of the circuit is acceptable good enough and can be use as control voltage for a very highly sensitive oscillator to vary its oscillating frequency in PLL. Circuit power dissipation mainly depends upon the supply voltage. By lowering the supply voltage and scaling the length and width of the CMOS at the appropriate proportion, the total circuit power dissipation is lowered without affecting the circuit performance.

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